AMENDMENTS TO THE CLAIMS

1-16. (Canceled)

17. (Previously Presented) An error correction method for an error correction code (ECC) block using a plurality of bytes of sub data which comprise error correction codes that are independent from error correction codes of an error correction target code line to configure erasure position information,

the plurality of bytes of sub data including at least a first byte of sub data and a second byte of sub data, said method comprising:

judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved;

configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judging judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved; and

performing error correction on the error correction target code line.

18. (Previously Presented) An error correction method for an error correction code (ECC) block using a plurality of bytes of sub data which comprise error correction codes that are independent from error correction codes of an error correction target code line to configure erasure position information,

the plurality of bytes of sub data including at least a first byte of sub data and a second byte of sub data, said method comprising:

judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the

first and second bytes of sub data before being deinterleaved;

configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judging judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved; and

performing error correction on the error correction target code line,

wherein the ECC block includes a plurality of main data areas comprising the plurality of bytes of main data of the error correction target code line and the plurality of bytes of main data of the previous error correction target code line, and a plurality of sub data areas comprising the plurality of bytes of sub data,

wherein the plurality of main data areas include a first main data area and a second main data area,

wherein the plurality of sub data areas include:

a first sub data area in which the first byte of sub data is located;

a second sub data area in which the second byte of sub data is located; and

a third sub data area in which a third byte of sub data is located,

wherein the first main data area is disposed between the first sub data area and the second sub data area,

wherein the second main data area is disposed between the second sub data area and the third sub data area,

wherein the second sub data area is disposed between the first main data area and the second main data area, and

wherein said error correction target code line extends so as to be located in both of the first and second main data areas of the ECC block before being deinterleaved.

19. (Currently Amended) An error correction method for an error correction code (ECC) block using a plurality of bytes of sub data which comprise error correction codes that are independent from error correction codes of an error correction target code line to configure

erasure position information,

the plurality of bytes of sub data including at least a first byte of sub data and a second byte of sub data, said method comprising:

judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved;

configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judging judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved; and

performing error correction on the error correction target code line,

~~An error correction method as defined in Claim 17,~~

wherein said configuring erasure position information of said first byte of main data utilizes sync data that is located in the ECC block at predetermined intervals.

20. (Previously Presented) An error correction method as defined in Claim 19, wherein said judging judges that the first byte of main data and the second byte of main data do not exist between the first and second bytes of sub data when said first byte of main data is directly subsequent to a byte of sub data or a byte of sync data in a data recording order.

21. (Previously Presented) An error correction method as defined in Claim 20, wherein said performing error correction performs error correction without using said erasure position information when an amount of said erasure position information configured in said configuring of erasure position information is higher than an amount of parity data.

22. (Previously Presented) An error correction method for an error correction code (ECC) block using a plurality of bytes of sub data which comprise error correction codes that are

independent from error correction codes of an error correction target code line to configure erasure position information,

the plurality of bytes of sub data including at least a first byte of sub data and a second byte of sub data, said method comprising:

judging whether or not a first byte of data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved when the previous error correction code line had error correction performed thereon by using said erasure position information;

configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judging judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved, and configuring erasure position information of every byte of main data of the error correction target code line when the previous error correction code line had error correction performed thereon without using erasure position information; and

performing error correction on the error correction target code line.

23. (Previously Presented) An error correction method for an error correction code (ECC) block using a plurality of bytes of sub data which comprise error correction codes that are independent from error correction codes of an error correction target code line to configure erasure position information,

the plurality of bytes of sub data including at least a first byte of sub data and a second byte of sub data, said method comprising:

judging whether or not a first byte of data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved when the previous error correction code line

had error correction performed thereon by using said erasure position information;

configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judging judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved, and configuring erasure position information of every byte of main data of the error correction target code line when the previous error correction code line had error correction performed thereon without using erasure position information; and

performing error correction on the error correction target code line,

wherein the ECC block includes a plurality of main data areas comprising the plurality of bytes of main data of the error correction target code line and the plurality of bytes of main data of the previous error correction target code line, and a plurality of sub data areas comprising the plurality of bytes of sub data,

wherein the plurality of main data areas include a first main data area and a second main data area,

wherein the plurality of sub data areas include:

a first sub data area in which the first byte of sub data is located;

a second sub data area in which the second byte of sub data is located; and

a third sub data area in which a third byte of sub data is located,

wherein the first main data area is disposed between the first sub data area and the second sub data area,

wherein the second main data area is disposed between the second sub data area and the third sub data area,

wherein the second sub data area is disposed between the first main data area and the second main data area, and

wherein said error correction target code line extends so as to be located in both of the first and second main data areas of the ECC block before being deinterleaved.

24. (Currently Amended) An error correction method for an error correction code (ECC) block using a plurality of bytes of sub data which comprise error correction codes that are independent from error correction codes of an error correction target code line to configure erasure position information,

the plurality of bytes of sub data including at least a first byte of sub data and a second byte of sub data, said method comprising:

judging whether or not a first byte of data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved when the previous error correction code line had error correction performed thereon by using said erasure position information;

configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judging judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved, and configuring erasure position information of every byte of main data of the error correction target code line when the previous error correction code line had error correction performed thereon without using erasure position information; and

performing error correction on the error correction target code line,

~~An error correction method as defined in Claim 22,~~

wherein said configuring erasure position information of said first byte of main data utilizes sync data that is located in the ECC block at predetermined intervals.

25. (Previously Presented) An error correction method as defined in Claim 24, wherein said judging judges that the first byte of data and the second byte of main data do not exist between the first and second bytes of sub data when said first byte of main data is directly subsequent to a byte of sub data or a byte of sync data in a data recording order.

26. (Previously Presented) An error correction method as defined in Claim 25, wherein said performing error correction performs error correction without using said erasure position information when an amount of said erasure position information configured in said configuring of erasure position information is higher than an amount of parity data.

27. (Previously Presented) An error correction apparatus for an error correction code (ECC) block using a plurality of bytes of sub data which comprise error correction codes that are independent from error correction codes of an error correction target code line to configure erasure position information,

the plurality of bytes of sub data including at least a first byte of sub data and a second byte of sub data, said apparatus comprising:

a judgment means for judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved;

a configuration means for configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judgment means judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved; and

an error correction means for performing error correction on the error correction target code line.

28. (Previously Presented) An error correction apparatus for an error correction code (ECC) block using a plurality of bytes of sub data which comprise error correction codes that are independent from error correction codes of an error correction target code line to configure erasure position information,

the plurality of bytes of sub data including at least a first byte of sub data and a second

byte of sub data, said apparatus comprising:

a judgment means for judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved;

a configuration means for configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judgment means judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved; and

an error correction means for performing error correction on the error correction target code line,

wherein the ECC block includes a plurality of main data areas comprising the plurality of bytes of main data of the error correction target code line and the plurality of bytes of main data of the previous error correction target code line, and a plurality of sub data areas comprising the plurality of bytes of sub data,

wherein the plurality of main data areas include a first main data area and a second main data area,

wherein the plurality of sub data areas include:

a first sub data area in which the first byte of sub data is located;

a second sub data area in which the second byte of sub data is located; and

a third sub data area in which a third byte of sub data is located,

wherein the first main data area is disposed between the first sub data area and the second sub data area,

wherein the second main data area is disposed between the second sub data area and the third sub data area,

wherein the second sub data area is disposed between the first main data area and the second main data area, and

wherein said error correction target code line extends so as to be located in both of the first and second main data areas of the ECC block before being deinterleaved.

29. (Currently Amended) An error correction apparatus for an error correction code (ECC) block using a plurality of bytes of sub data which comprise error correction codes that are independent from error correction codes of an error correction target code line to configure erasure position information,

the plurality of bytes of sub data including at least a first byte of sub data and a second byte of sub data, said apparatus comprising:

a judgment means for judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved;

a configuration means for configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judgment means judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved; and

an error correction means for performing error correction on the error correction target code line,

~~An error correction apparatus as defined in Claim 27,~~

wherein said configuration means for configuring erasure position information of said first byte of main data utilizes sync data that is located in the ECC block at predetermined intervals.

30. (Currently Amended) An error correction apparatus for an error correction code (ECC) block using a plurality of bytes of sub data which comprise error correction codes that are independent from error correction codes of an error correction target code line to configure

erasure position information,

the plurality of bytes of sub data including at least a first byte of sub data and a second byte of sub data, said apparatus comprising:

a judgment means for judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved;

a configuration means for configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judgment means judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved; and

an error correction means for performing error correction on the error correction target code line,

wherein said configuration means for configuring erasure position information of said first byte of main data utilizes sync data that is located in the ECC block at predetermined intervals, and

~~An error correction apparatus as defined in Claim 29,~~

wherein said judgment means judges that said first byte of main data and said second byte of main data do not exist between the first and second bytes of sub data when said first byte of main data is directly subsequent to a byte of sub data or a byte of sync data in a data recording order.

31. (Currently Amended) An error correction apparatus for an error correction code (ECC) block using a plurality of bytes of sub data which comprise error correction codes that are independent from error correction codes of an error correction target code line to configure erasure position information,

the plurality of bytes of sub data including at least a first byte of sub data and a second

byte of sub data, said apparatus comprising:

a judgment means for judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved;

a configuration means for configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judgment means judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved; and

an error correction means for performing error correction on the error correction target code line,

wherein said configuration means for configuring erasure position information of said first byte of main data utilizes sync data that is located in the ECC block at predetermined intervals,

wherein said judgment means judges that said first byte of main data and said second byte of main data do not exist between the first and second bytes of sub data when said first byte of main data is directly subsequent to a byte of sub data or a byte of sync data in a data recording order, and

~~An error correction apparatus as defined in Claim 30,~~

wherein said error correction means performs error correction without using said erasure position information when an amount of said erasure position information configured by said configuration means is higher than an amount of parity data.

32. (Previously Presented) An error correction apparatus for an error correction code (ECC) block using a plurality of bytes of sub data which comprise error correction codes that are independent from error correction codes of an error correction target code line to configure erasure position information,

the plurality of bytes of sub data including at least a first byte of sub data and a second byte of sub data, said apparatus comprising:

a judgment means for judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved when the previous error correction code line had error correction performed thereon by using said erasure position information;

a configuration means for configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judgment means judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved, and configuring erasure position information of every byte of main data of the error correction target code line when the previous error correction code line had error correction performed thereon without using erasure position information; and

an error correction means for performing error correction on the error correction target code line.

33. (Previously Presented) An error correction apparatus for an error correction code (ECC) block using a plurality of bytes of sub data which comprise error correction codes that are independent from error correction codes of an error correction target code line to configure erasure position information,

the plurality of bytes of sub data including at least a first byte of sub data and a second byte of sub data, said apparatus comprising:

a judgment means for judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved when the

previous error correction code line had error correction performed thereon by using said erasure position information;

a configuration means for configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judgment means judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved, and configuring erasure position information of every byte of main data of the error correction target code line when the previous error correction code line had error correction performed thereon without using erasure position information; and

an error correction means for performing error correction on the error correction target code line,

wherein the ECC block includes a plurality of main data areas comprising the plurality of bytes of main data of the error correction target code line and the plurality of bytes of main data of the previous error correction target code line, and a plurality of sub data areas comprising the plurality of bytes of sub data,

wherein the plurality of main data areas include a first main data area and a second main data area,

wherein the plurality of sub data areas include:

a first sub data area in which the first byte of sub data is located;

a second sub data area in which the second byte of sub data is located; and

a third sub data area in which a third byte of sub data is located,

wherein the first main data area is disposed between the first sub data area and the second sub data area,

wherein the second main data area is disposed between the second sub data area and the third sub data area,

wherein the second sub data area is disposed between the first main data area and the second main data area, and

wherein said error correction target code line extends so as to be located in both of the

first and second main data areas of the ECC block before being deinterleaved.

34. (Currently Amended) An error correction apparatus for an error correction code (ECC) block using a plurality of bytes of sub data which comprise error correction codes that are independent from error correction codes of an error correction target code line to configure erasure position information,

the plurality of bytes of sub data including at least a first byte of sub data and a second byte of sub data, said apparatus comprising:

a judgment means for judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved when the previous error correction code line had error correction performed thereon by using said erasure position information;

a configuration means for configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judgment means judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved, and configuring erasure position information of every byte of main data of the error correction target code line when the previous error correction code line had error correction performed thereon without using erasure position information; and

an error correction means for performing error correction on the error correction target code line,

~~An error correction apparatus as defined in Claim 32,~~

wherein said configuration means for configuring erasure position information of said first byte of main data utilizes sync data that is located in the ECC block at predetermined intervals.

35. (Currently Amended) An error correction apparatus for an error correction code (ECC) block using a plurality of bytes of sub data which comprise error correction codes that are independent from error correction codes of an error correction target code line to configure erasure position information,

the plurality of bytes of sub data including at least a first byte of sub data and a second byte of sub data, said apparatus comprising:

a judgment means for judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved when the previous error correction code line had error correction performed thereon by using said erasure position information;

a configuration means for configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judgment means judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved, and configuring erasure position information of every byte of main data of the error correction target code line when the previous error correction code line had error correction performed thereon without using erasure position information; and

an error correction means for performing error correction on the error correction target code line,

wherein said configuration means for configuring erasure position information of said first byte of main data utilizes sync data that is located in the ECC block at predetermined intervals, and

~~An error correction apparatus as defined in Claim 34,~~

wherein said judgment means judges that said first byte of main data and said second byte of main data do not exist between the first and second bytes of sub data when said first byte of main data is directly subsequent to a byte of sub data or a byte of sync data in a data recording

order.

36. (Currently Amended) An error correction apparatus for an error correction code (ECC) block using a plurality of bytes of sub data which comprise error correction codes that are independent from error correction codes of an error correction target code line to configure erasure position information,

the plurality of bytes of sub data including at least a first byte of sub data and a second byte of sub data, said apparatus comprising:

a judgment means for judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved when the previous error correction code line had error correction performed thereon by using said erasure position information;

a configuration means for configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judgment means judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved, and configuring erasure position information of every byte of main data of the error correction target code line when the previous error correction code line had error correction performed thereon without using erasure position information; and

an error correction means for performing error correction on the error correction target code line,

wherein said configuration means for configuring erasure position information of said first byte of main data utilizes sync data that is located in the ECC block at predetermined intervals,

wherein said judgment means judges that said first byte of main data and said second byte of main data do not exist between the first and second bytes of sub data when said first byte of

main data is directly subsequent to a byte of sub data or a byte of sync data in a data recording order, and

~~An error correction apparatus as defined in Claim 35,~~

wherein said error correction means performs error correction without using said erasure position information when an amount of said erasure position information configured by said configuration means is higher than an amount of parity data.

37. (Currently Amended) An error correction method for an error correction code (ECC) block using a plurality of bytes of sub data which comprise error correction codes that are independent from error correction codes of an error correction target code line to configure erasure position information,

the plurality of bytes of sub data including at least a first byte of sub data and a second byte of sub data, said method comprising:

judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved;

configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judging judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved; and

performing error correction on the error correction target code line,

wherein the ECC block includes a plurality of main data areas comprising the plurality of bytes of main data of the error correction target code line and the plurality of bytes of main data of the previous error correction target code line, and a plurality of sub data areas comprising the plurality of bytes of sub data,

wherein the plurality of main data areas include a first main data area and a second main data area,

wherein the plurality of sub data areas include:

a first sub data area in which the first byte of sub data is located;

a second sub data area in which the second byte of sub data is located; and

a third sub data area in which a third byte of sub data is located,

wherein the first main data area is disposed between the first sub data area and the second sub data area,

wherein the second main data area is disposed between the second sub data area and the third sub data area,

wherein the second sub data area is disposed between the first main data area and the second main data area,

wherein said error correction target code line extends so as to be located in both of the first and second main data areas of the ECC block before being deinterleaved, and

~~An error correction method as defined in Claim 18,~~

wherein said configuring erasure position information of said first byte of main data utilizes sync data that is located in the ECC block at predetermined intervals.

38. (Currently Amended) An error correction method for an error correction code (ECC) block using a plurality of bytes of sub data which comprise error correction codes that are independent from error correction codes of an error correction target code line to configure erasure position information,

the plurality of bytes of sub data including at least a first byte of sub data and a second byte of sub data, said method comprising:

judging whether or not a first byte of data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved when the previous error correction code line had error correction performed thereon by using said erasure position information;

configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte

of main data belonging to the previous error correction code line when said judging judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved, and

configuring erasure position information of every byte of main data of the error correction target code line when the previous error correction code line had error correction performed thereon without using erasure position information; and

performing error correction on the error correction target code line,

wherein the ECC block includes a plurality of main data areas comprising the plurality of bytes of main data of the error correction target code line and the plurality of bytes of main data of the previous error correction target code line, and a plurality of sub data areas comprising the plurality of bytes of sub data,

wherein the plurality of main data areas include a first main data area and a second main data area,

wherein the plurality of sub data areas include:

a first sub data area in which the first byte of sub data is located;

a second sub data area in which the second byte of sub data is located; and

a third sub data area in which a third byte of sub data is located,

wherein the first main data area is disposed between the first sub data area and the second sub data area,

wherein the second main data area is disposed between the second sub data area and the third sub data area,

wherein the second sub data area is disposed between the first main data area and the second main data area,

wherein said error correction target code line extends so as to be located in both of the first and second main data areas of the ECC block before being deinterleaved, and

~~An error correction method as defined in Claim 23,~~

wherein said configuring erasure position information of said first byte of main data utilizes sync data that is located in the ECC block at predetermined intervals.

39. (Currently Amended) An error correction apparatus for an error correction code (ECC) block using a plurality of bytes of sub data which comprise error correction codes that are independent from error correction codes of an error correction target code line to configure erasure position information,

the plurality of bytes of sub data including at least a first byte of sub data and a second byte of sub data, said apparatus comprising:

a judgment means for judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved;

a configuration means for configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judgment means judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved; and

an error correction means for performing error correction on the error correction target code line,

wherein the ECC block includes a plurality of main data areas comprising the plurality of bytes of main data of the error correction target code line and the plurality of bytes of main data of the previous error correction target code line, and a plurality of sub data areas comprising the plurality of bytes of sub data,

wherein the plurality of main data areas include a first main data area and a second main data area,

wherein the plurality of sub data areas include:

a first sub data area in which the first byte of sub data is located;

a second sub data area in which the second byte of sub data is located; and

a third sub data area in which a third byte of sub data is located,

wherein the first main data area is disposed between the first sub data area and the second

sub data area,

wherein the second main data area is disposed between the second sub data area and the third sub data area,

wherein the second sub data area is disposed between the first main data area and the second main data area,

wherein said error correction target code line extends so as to be located in both of the first and second main data areas of the ECC block before being deinterleaved, and

~~An error correction apparatus as defined in Claim 28,~~

wherein said configuration means for configuring erasure position information of said first byte of main data utilizes sync data that is located in the ECC block at predetermined intervals.

40. (Currently Amended) An error correction apparatus for an error correction code (ECC) block using a plurality of bytes of sub data which comprise error correction codes that are independent from error correction codes of an error correction target code line to configure erasure position information,

the plurality of bytes of sub data including at least a first byte of sub data and a second byte of sub data, said apparatus comprising:

a judgment means for judging whether or not a first byte of main data, which is one of a plurality of bytes of main data of the error correction target code line, and a second byte of main data, which is one of a plurality of bytes of main data of a previous error correction code line, were located between the first and second bytes of sub data before being deinterleaved when the previous error correction code line had error correction performed thereon by using said erasure position information;

a configuration means for configuring erasure position information of said first byte of main data belonging to the error correction target code line to be identical to erasure position information of said second byte of main data belonging to the previous error correction code line when said judgment means judges that the first byte of main data and the second byte of main data were both located between the first and second bytes of sub data before being deinterleaved,

and configuring erasure position information of every byte of main data of the error correction target code line when the previous error correction code line had error correction performed thereon without using erasure position information; and

an error correction means for performing error correction on the error correction target code line,

wherein the ECC block includes a plurality of main data areas comprising the plurality of bytes of main data of the error correction target code line and the plurality of bytes of main data of the previous error correction target code line, and a plurality of sub data areas comprising the plurality of bytes of sub data,

wherein the plurality of main data areas include a first main data area and a second main data area,

wherein the plurality of sub data areas include:

a first sub data area in which the first byte of sub data is located;

a second sub data area in which the second byte of sub data is located; and

a third sub data area in which a third byte of sub data is located,

wherein the first main data area is disposed between the first sub data area and the second sub data area,

wherein the second main data area is disposed between the second sub data area and the third sub data area,

wherein the second sub data area is disposed between the first main data area and the second main data area,

wherein said error correction target code line extends so as to be located in both of the first and second main data areas of the ECC block before being deinterleaved, and

~~An error correction apparatus as defined in Claim 33,~~

wherein said configuration means for configuring erasure position information of said first byte of main data utilizes sync data that is located in the ECC block at predetermined intervals.